

What is claimed is:

1 1. A precharge system, appropriate for an active
2 matrix display device having a plurality of data lines, a
3 plurality of scan lines, a plurality of pixels, a first
4 voltage source, and a second voltage source, comprising a
5 precharge circuit having:

6 a plurality of first transistors, having gate electrode
7 and drain electrode connected together to
8 function as a diode, of which a first terminal is
9 coupled to the first voltage source;

10 a second transistor of which a first terminal is
11 coupled to the second terminals of the first
12 transistors, of which a second terminal is
13 coupled to the data lines, and a control terminal
14 receives a positive precharge signal;

15 a plurality of third transistors, having gate electrode
16 and drain electrode connected together to
17 function as a diode, of which a first terminal is
18 coupled to the second voltage source; and

19 a fourth transistor of which a first terminal is
20 coupled to the second terminals of the third
21 transistors, of which a second terminal is
22 coupled to the corresponding data lines, and a
23 control terminal receives a negative precharge
24 signal.

1 2. The precharge system as claimed in claim 1,
2 wherein the first transistors are N-type thin film
3 transistors.

1 3. The precharge system as claimed in claim 1,
2 wherein the second transistor is an N-type thin film
3 transistor.

1 4. The precharge system as claimed in claim 1,
2 wherein the second transistor is a P-type thin film
3 transistor.

1 5. The precharge system as claimed in claim 1,
2 wherein the third transistors are N-type thin film
3 transistors.

1 6. The precharge system as claimed in claim 1,
2 wherein the third transistors are P-type thin film
3 transistors.

1 7. The precharge system as claimed in claim 1,
2 wherein the first transistors are P-type thin film
3 transistors.

1 8. The precharge system as claimed in claim 1 further
2 comprising a plurality of precharge circuits coupled to the
3 corresponding data lines.

1 9. The precharge system as claimed in claim 8 further
2 comprising a control signal generation circuit for
3 generating the positive precharge signal and the negative
4 precharge signal.

1 10. The precharge system as claimed in claim 9,
2 wherein the control signal generation circuit comprises:

3 a selection circuit having an input terminal, a
4 selection terminal, a complementary selection
5 terminal, a first output terminal, and a second
6 output terminal, wherein the input terminal
7 receives a start impulse signal and the selection
8 terminal and the complementary selection terminal
9 enable the first output terminal or the second
10 output terminal; and
11 a voltage level shifter for receiving a clock signal
12 and a complementary clock signal and for coupling
13 the clock signal and the complementary clock
14 signal respectively to the selection terminal and
15 to the complementary selection terminal.

1 11. The precharge system as claimed in claim 9,
2 wherein the control signal generation circuit comprises:
3 a selection circuit having an input terminal, a
4 selection terminal, a complementary selection
5 terminal, a first output terminal, and a second
6 output terminal, wherein the input terminal
7 receives a start impulse signal and wherein the
8 selection terminal and the complementary
9 selection terminal enable the first output
10 terminal or the second output terminal; and
11 a voltage level shifter for receiving the common
12 voltage signal and coupling the amplified common
13 voltage signal and the complementary amplified
14 common voltage signal respectively to the
15 selection terminal and to the complementary
16 selection terminal.

17 an inverter of which an input terminal is coupled to
18 the output terminal of the voltage level shifter
19 and an output terminal is coupled to the
20 complementary selection terminal.

1 12. The precharge system as claimed in claim 11,
2 wherein the selection circuit comprises:

3 a first transmission gate having a first terminal and a
4 second terminal, wherein the first terminal is
5 coupled to the input terminal and wherein a first
6 gate of the second terminal is coupled to the
7 selection terminal, and a second gate of the
8 second terminal is coupled to the complementary
9 selection terminal;

10 a third transistor having a first terminal coupled to
11 the second terminal of the first transmission
12 gate, having a second terminal coupled to a low
13 voltage source, and having a control terminal
14 coupled to the selection terminal;

15 a second transmission gate having a first terminal and
16 a second terminal, wherein the first terminal is
17 coupled to the input terminal and wherein a first
18 gate of the second terminal is coupled to the
19 complementary selection terminal, and a second
20 gate of the second terminal is coupled to the
21 selection terminal; and

22 a fourth transistor having a first terminal coupled to
23 the second terminal of the second transmission
24 gate, having a second terminal coupled to the low

25 voltage source, and having a control terminal
26 coupled to the complementary selection terminal.

1 13. The precharge system as claimed in claim 8 further
2 comprising a plurality of control signal generation circuits
3 for respectively generating the positive precharge signal
4 and the negative precharge signal and for coupling the
5 positive precharge signal and the negative precharge signal
6 to the corresponding precharge circuits.